UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,921	02/20/2004	Tadayuki Taura	001701.00201	5313

22907 7590 06/07/2004

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,921	TAURA ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication app ars on th cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02-16-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/230,704, now Patent No. 6,711,057, filed on 09/05/2002.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 02/20/2004 is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (U.S. Pat. No. 5,841,711).

Regarding claim 1, Watanabe discloses a semiconductor memory device comprising: a first nonvolatile storage (figure 6, latch flag circuit) configured to store semiconductor chip codes of semiconductor chips; a latch circuit (figure 6, address latch circuit) configured to latch an address upon receipt of an activating signal; and a first comparator circuit (figure 6, comparator circuit 10) configured to compare a semiconductor chip code inputted from an external source with the semiconductor chip codes stored in the first storage, and output the activating signal when the inputted chip code coincides with one of the stored chip codes

(comparator circuit 10 compare the chip code from the DQ buffer and the one from the memory array, col. 5, lines 7+).

Regarding claims 2 and 8, Watanabe discloses the semiconductor memory device according to claim 1, further comprising: a write control circuit (figure 6, nonvolatile latch write control circuit) configured to generate a write signal; and a second nonvolatile storage (figure 5, second nonvolatile latch) configured to store the address latched by the latch circuit upon receipt of the write signal (col. 5, lines 7+).

Regarding claims 3 and 9, Watanabe discloses the semiconductor memory device according to claim 2, further comprising: a first memory cell array (figure 6, memory array 8) formed of a plurality of memory cells; a second memory cell array formed of a plurality of redundancy cells (figure 6, nonvolatile redundancy storage latch circuit); an address buffer (figure 6, address buffer 1 and 2) configured to receive an input address; a second comparator circuit configured to compare the input address of the address buffer with the address stored in the second storage, and output an output signal denoting a coincidence/non-coincidence thereof; and an output multiplexer configured to receive the output signal of the second comparator circuit and select data read out from one of the first and second memory cell arrays in accordance with the coincidence/non-coincidence denoted by the output signal of the second comparator circuit (compare circuit in the control circuit 3, col. 5, lines 20+; col. 6, lines 18+).

Regarding claims 4 and 10, Watanabe disclose the semiconductor memory device according to claim 1, in which the first storage comprises memory cells in which the chip codes are re-storable (col. 5, lines 8+).

Regarding claims 5 and 11, Watanabe discloses the semiconductor memory device according to claim 2, in which the first storage comprises memory cells in which the chip codes are re-storable (col. 5, lines 8+).

Regarding claims 6 and 12, Watanabe discloses the semiconductor memory device according to claim 3, in which the first storage comprises the memory cells in which the chip codes are re-storable (col. 5, lines 8+).

Regarding claim 7, Watanabe discloses the semiconductor memory device according to claim 3, in which the second storage comprises the memory cells having a structure the same as the memory cells of the memory cell array, in which the address is re-storable (col. 5, lines 8+).

Regarding claim 13, Watanabe discloses the semiconductor memory device according to claim 1, in which the address latched by the latch circuit is an address of an area of a storing portion of each of the semiconductor chips, which area is faulty (col. 5, lines 20+).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
May 21, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818